FIG. 2(a) Current art SRAM operation

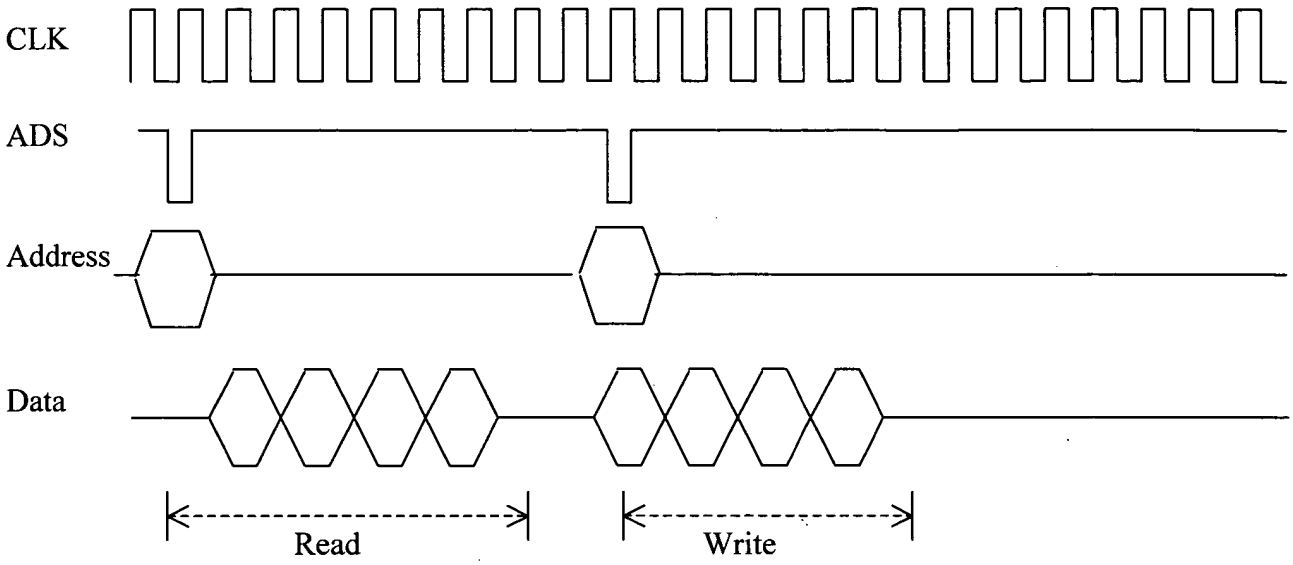

FIG. 2(b) Current art DRAM operation